WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Tuesday, August 17, 2004

Hide?	Set Name	Query	Hit Count
		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L40	l27 and (trigger$4 near5 control$4)	3
☐	L39	L38 same power	1
☐	L38	(mode near3 track$4 near3 status)	38
☐	L37	(mode near3 track$4)	9357
☐	L36	l1 and L34	2
☐	L35	l22 and L34	0
☐	L34	((plurality or multiple) near3 power near3 control$4 near3 mechanism)	57
☐	L33	l1 and l27	7
☐	L32	l2 and l27	0
☐	L31	l7 and l27	0
☐	L30	l7 and l22	0
☐	L29	l5 and l22	1
☐	L28	l22 and L27	6
☐	L27	((multiple or plurality) near2 modes) and (power near3 throttl$4)	41
☐	L26	((multiple or plurality) near2 modes) same (power near3 throttl$4)	5
☐	L25	l5 and L23	0
☐	L24	l7 and L23	0
☐	L23	l2 and L22	14
☐	L22	l16 or l17 or l18 or l19 or l20 or L21	2449
☐	L21	710/18.ccls.	287
☐	L20	710/15.ccls.	437
☐	L19	713/340.ccls.	449
☐	L18	713/321.ccls.	521
☐	L17	713/320.ccls.	564
☐	L16	713/300.ccls.	870
☐	L15	"WO 9917186 A"	0
☐	L14	"WO 9917186 A".pn.	0
☐	L13	9917186.pn.	2
☐	L12	WO9917186A.pn.	0
☐	L11	WO9917186A	0
☐	L10	5719800.pn.	2

☐	L9	l2.clm.	7
☐	L8	l5 same L6	7
☐	L7	l5 and L6	13
☐	L6	(activat$4 near2 second near2 power near2 control$4)	37
☐	L5	(activat$4 near2 first near2 power near2 control$4)	51
☐	L4	L2 and (activat$4 near3 power near3 control$4)	2
☐	L3	L2 same (activat$4 near3 power near3 control$4)	0
☐	L2	L1 same (determin$4 near3 power near3 state)	90
☐	L1	((monitor$4 or snoop$4) near5 (activity or state))	65455

END OF SEARCH HISTORY

L28: Entry 2 of 6 File: USPT Jun 3, 2003

DOCUMENT-IDENTIFIER: US 6574740 B1
TITLE: Dynamic power consumption control for a computer or other electronic apparatus

Brief Summary Text (12):
Power consumption of an electronic apparatus such as a computer or the like varies in accordance with a type of its processed data or an operating state. This invention may be applied to an electronic apparatus, which includes a load with its power consumption being adjustable (hereinafter called "controlled load") and a set of loads comprising a plurality of components (hereinafter called "base loads"). The controlled load has a plurality of operation modes corresponding to functional levels in such a manner that when the operation modes are switched or changed from one to another, maximum power consumption of the controlled load and its actual power consumption are varied accordingly. On the other hand, actual power consumption of the base loads is, in general, far less than a sum of maximum power consumption of each component, and this power consumption varies as a result of a change in an operating state of the electronic apparatus.

Brief Summary Text (13):
In one aspect of this invention, there is provided a method of controlling power consumption of a computer, which is provided with base loads comprising a plurality of components, and a CPU including a plurality of operation modes associated with power consumption thereof, the method comprising the steps of: obtaining predicted maximum power consumption of said computer from actual power consumption of said base loads and maximum power consumption in a current operation mode of said CPU; providing reference power; comparing said predicted maximum power consumption with said reference power; and changing the operation mode of said CPU in response to said comparing step. It is clear from the description of the present specification, however, that application of this invention is not limited to controlling of power consumption of a computer, since this invention is broadly applicable to controlling of power consumption of a conventional electronic apparatus as well. Also, the load including a plurality of operation modes associated with power consumption thereof is not limited to a CPU alone, since it may be any load so long as its power consumption is changeable, i.e., any member of the so-called "controlled loads". Note here that the expression, "operation modes associated with power consumption", refers to one or more operation modes of intermediate states (each being capable of consuming a certain amount of power) between the most active operation mode (wherein the controlled load consumes its maximum power) and the most inactive operation mode (wherein the controlled load is stopped), and that upon setting one of the operation modes, maximum power consumption in this operation mode so set up is determined, thereby to confine its actual power consumption within the said maximum power consumption.

Brief Summary Text (14):
A CPU runs in synchronization with timing of clocks. Thus, a program can be executed even if clocks are not successively sent at a predetermined frequency. Recognizing such behavior, there has been developed a known technique of an operation mode, called "throttling", for controlling power consumption and/or a temperature rise by periodically stopping clocks of the CPU for a predetermined time interval. Changing a duty cycle of the throttling, maximum power consumption

L28: Entry 4 of 6 File: USPT Nov 9, 1999

DOCUMENT-IDENTIFIER: US 5983356 A
TITLE: Power conservation method and apparatus activated by detecting shadowed interrupt signals indicative of system inactivity and excluding prefetched signals

Brief Summary Text (15):
To overcome the limitations of the prior art, the present invention is embodied in a system controller disposed within a computer system which receives signals including address signals, signals indicative of primary and secondary activity, and at least one nap timeout signal. Addresses which match shadowed addresses trigger the generation of a nap signal. The nap signal may be applied to a stop clock state machine which generates a clock stopping signal. The clock stopping signal is applied to the processor to suspend processing. A plurality of mode timers determine when the computer system may be advanced to a progressively lower power mode. Any primary or secondary activity may be applied to the logic circuit resulting in the deassertion of the nap signal in one of at least two modes. Deassertion of the nap signal results in the clock stopping signal being removed. Full speed processing resumes upon removal of the clock stopping signal in certain instances.

Current US Cross Reference Classification (1):
713/320

CLAIMS:

22. A power conservation circuit comprising:

a nap triggering circuit receiving a first signal and generating a second signal when the first signal is indicative of system inactivity, the nap triggering circuit comprising a first shadow register receiving and storing a first shadowed address, a first logic block receiving the first signal and trapping the first signal into a second shadowed address, and a comparison block coupled to the first shadow register and to the first logic block, the comparison block receiving and comparing the first shadowed address with the second shadowed address and generating the second signal if the second address matches the first shadowed address;

a prefetch detect circuit receiving the first signal and generating a third signal when the first signal is the product of a prefetch cycle; and

a throttling circuit coupled to the nap triggering circuit and to the prefetch detect circuit, the throttling circuit generating a clock stopping signal upon receipt of the second signal but not generating a clock stopping signal upon receipt of the third signal, such that communication of the clock stopping signal to a system clock results in inhibition of the system clock and power conservation, the throttling circuit comprising a first register for storing a first value corresponding to a duration of a time period, a second register for storing a second value corresponding to a duty cycle of the clock stopping signal, and a logic block, coupled to the first and second registers, for receiving the first and second values and the second signal, the logic block enabling the throttling circuit to apply the clock stopping signal in response to the second signal and

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#
Generate Collection Print

L23: Entry 1 of 14 File: USPT Jul 6, 2004

DOCUMENT-IDENTIFIER: US 6760850 B1
TITLE: Method and apparatus executing power on self test code to enable a wakeup device for a computer system responsive to detecting an AC power source

Brief Summary Text (12):
Early implementations of the various power modes required the computer hardware itself to monitor user activity and determine the proper power state for each device in the computer system. These early computer systems included a read only memory (ROM) device that stored a set of instructions for the computer to follow in order to carry out power management functions. The set of instructions formed part of the Basic Input/Output System (BIOS) of the computer, which also included instructions for procedures such as accessing data on a hard or floppy disk drive and controlling the graphics display. The ROM device containing the BIOS is referred to as the "BIOS ROM". Because hardware-based power management instructions usually are included in BIOS, such a management scheme is commonly known as "BIOS power management". Under BIOS power management, conditions within the computer system that initiate power state transitions, such as button presses and periods of inactivity explained above, generate system management interrupt (SMI) signals to the central processing unit (CPU). Upon receiving an SMI, the CPU executes the BIOS power management instructions stored in ROM to change the power state.

Current US Original Classification (1):
713/320

Current US Cross Reference Classification (1):
713/300

Current US Cross Reference Classification (6):
713/340

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#
Generate Collection Print

L23: Entry 7 of 14 File: USPT Jun 5, 2001

DOCUMENT-IDENTIFIER: US 6243817 B1
TITLE: Device and method for dynamically reducing power consumption within input buffers of a bus interface unit

Brief Summary Text (16):
The present mechanism can also monitor the power state of the computer to determine if the computer is in a run state or a sleep state. If in a sleep state (including, e.g., idle state, standby state and hibernation state), then the CPU bus is monitored for a stop clock signal (STPCLK_) which indicates entry into the sleep state. If the stop clock signal is encountered, then all input buffers and/or differential amplifiers coupled to receive input signals from the CPU bus are disconnected from power. As defined herein below, power is the upper or lower power supplies, including V.sub.DD, V.sub.CC and/or ground.

Current US Original Classification (1):
713/300

Current US Cross Reference Classification (5):
713/340

Previous Doc Next Doc Go to Doc#

L9: Entry 7 of 7 File: USPT Jun 16, 1981

DOCUMENT-IDENTIFIER: US 4274132 A
TITLE: Power supply arrangements

CLAIMS:

1. A power supply arrangement in which a power source is connected to supply a load which requires varying amounts of electrical power, and comprising reservoir storage means for receiving a variable level of electrical energy from said source, charge control circuit means connected between said reservoir storage means and said source for varying the level of electrical energy transferred to said storage means, discharge control circuit means connected between said storage means and the load for supplying the load with the varying amounts of electrical power required thereby, and processor means, having a first input connected to said source, a second input connected to said storage means, a first output connected to said charge control circuit means and a second output connected to said discharge control circuit means, and programmed to monitor the state of said power source to determine its capability for providing power to said reservoir storage means and to control said charge control circuit to achieve optimum charging thereof and to control said discharge control circuit to supply power to said load as required and consistent with the state of charge of said reservoir storage means and the capability of said power source.

4. A power supply arrangement in which a power source is connected to supply a load and comprising reservoir storage means arranged to be charged via a charge control circuit from said source and to supply said load via a discharge control circuit and a processor programmed and arranged to monitor the state of said power source to determine its capability for providing power to said reservoir storage means and to control said charge control circuit to achieve optimum charging thereof and to control said discharge control circuit to supply power to said load as required and consistent with the state of charge of said reservoir storage means and the capability of said power source, said power source being connected to supply power to auxiliary equipments, and said processor being arranged to control the operation of an auxiliary and to switch this off where the power supplied thereto is required for said load and circumstances permit.

6. A power supply arrangement in which a power source is connected to supply a load and comprising reservoir storage means arranged to be charged via a charge control circuit from said source and to supply said load via a discharge control circuit and a processor programmed and arranged to monitor the state of said power source to determine its capability for providing power to said reservoir storage means and to control said charge control circuit to achieve optimum charging thereof and to control said discharge control circuit to supply power to said load as required and consistent with the state of charge of said reservoir storage means and the capability of said power source, said processor being arranged to control said charge control circuit in such manner that power is supplied to said load, or the power level of the power supplied to said load is increased, in pulse form, said processor being arranged to control the amount of energy in a pulse and/or the pulse repetition rate and/or pattern in dependence upon the tasks to be performed

L9: Entry 6 of 7 File: USPT Jul 26, 1994

DOCUMENT-IDENTIFIER: US 5333176 A
TITLE: Cellular hand held portable speakerphone system having an interface adapter

CLAIMS:

1. An apparatus, comprising:

a cellular telephone including a telephone microphone, a telephone speaker, receiver means for receiving analog signals and digital signals from a base station, transmitter means for transmitting analog signals and digital signals to the base station, a battery pack configured to be mounted within the cellular telephone, the battery pack including a power source, switch means for electrically coupling the power source and the cellular telephone, the switch means configured to be turned off and on, battery state monitoring means for continuously monitoring a state of charge of the power source, determining means, responsive tot he state of charge of the power source, for determining an amount of time remaining for use of the battery pack based on the state of charge, and display means, responsive to the control means, for providing a real time display of the time remaining for use of the battery pack;

interface means for supporting the cellular telephone in at least a locked position and an unlocked position, the interface means including power supply means for supplying power to the cellular telephone when the cellular telephone is being supported by the interface means, an interface microphone, an interface speaker, each of the interface microphone and the interface speaker being operably connected tot he cellular telephone when the cellular telephone is supported by the interface means, the receiver means and the interface speaker defining a receive path, and the transmitter means and one of the telephone microphone and the interface microphone defining a transmit path;

power control means for controlling the switch means to be turned on when the cellular telephone is in the unlocked position and turned off when the cellular telephone is in the locked position;

converter means for converging analog signals received from each of the telephone microphone, the interface microphone and the receiver means into digital signals;

sampling means for sampling digital signals on each of the transmit path and the receive path and for storing values corresponding to a predetermined characteristic of the samples digital signals;

determining means for determining an energy value for the digital signals on each of the transmit path and the receive path over a predetermined period based on the stored values of the predetermined characteristic;

switching means for switching off one of the transmit path and the receive path in response to the determined energy values;

memory means for storing digital signals;

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

End of Result Set

Generate Collection Print

L8: Entry 7 of 7 File: USPT Apr 4, 1989

DOCUMENT-IDENTIFIER: US 4817466 A
TITLE: Remote control system for marine engine

CLAIMS:

11. In a remote control system for a watercraft having a propulsion unit comprising an engine having an engine speed control and a transmission having at least a forward gear, a reverse gear and a neutral, first power means for moving said engine speed control between an idle position, a part throttle position and a full throttle position, second power means for moving said transmission between said forward gear, said neutral and said reverse gear conditions, a remote control device for activating said first and second power means, and computer means for transmitting signals from said remote control device to said first and second power means including logic for precluding said first power means from moving said engine speed control past the part throttle position when the transmission is in a predetermined one of its conditions.

13. In a remote control system for a watercraft having a propulsion unit comprising an engine having an engine speed control and a transmission having at least a forward gear, a reverse gear and a neutral, first power means for moving said engine speed control between an idle position, a part throttle position and a full throttle position, second power means for moving said transmission between said forward gear, said neutral and said reverse gear conditions, a remote control device for activating said first and second power means, and computer means for transmitting signals from said remote control device to said first and second power means including logic for rapidly reducing the throttle valve position and shifting the transmission from one of its positions through neutral to the other of its positions in response to an emergency deceleration signal.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#
Generate Collection Print

L9: Entry 1 of 7 File: USPT Apr 24, 2001

DOCUMENT-IDENTIFIER: US 6222347 B1
**** See image for Certificate of Correction ****
TITLE: System for charging portable computer's battery using both the dynamically determined power available based on power consumed by sub-system devices and power limits from the battery

CLAIMS:

15. A computer system, comprising:

a power supply for providing DC power to said computer system from an AC power source;

a battery for providing DC power to said computer system;

a plurality of peripheral subsystems, each of the peripheral subsystems having a low-power state and an active state;

a processor for performing computations and controlling said computer system;

a power management unit for monitoring status of said battery, monitoring the state of said peripheral subsystems, and determining an amount of power available for charging based at least in part on those of said peripheral subsystems that are in the inactive state; and

a battery charge circuit for delivering power from said power supply to said battery in accordance with the amount of power available for charging

wherein said power management unit monitors of the status of said battery by monitoring a power limit for charging said battery and the amount of power available for charging is limited by the power limit.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#
Generate Collection Print

L9: Entry 2 of 7 File: USPT Mar 14, 2000

DOCUMENT-IDENTIFIER: US 6038515 A
TITLE: Portable information terminal apparatus capable of correctly detecting power supply voltage

CLAIMS:

1. A portable information terminal system including a CPU and peripheral circuits, comprising:

a power supply;

a discharge quantity table for storing remaining power levels, each of which is defined based on a system state of said portable information terminal system and a voltage of said power supply;

a voltage detecting unit for detecting said power supply voltage in response to a voltage detection request; and

a control section for monitoring said system state, for issuing said voltage detection request in response to a voltage check request, for referring to said discharge quantity table based on said power supply voltage detected by said voltage detecting unit and said monitored system state to determine said remaining power level of said power supply.

11. A method of determining a remaining power level of a power supply in a portable information terminal system including a CPU and peripheral circuits, comprising the steps of:

monitoring a system state of the portable information terminal system;

issuing a voltage detection request in response to a voltage check request;

detecting a power supply voltage in response to said voltage detection request; and

referring to a discharge quantity table based on said power supply voltage detected by said voltage detecting unit and said monitored system state to determine said remaining power level of said power supply, wherein said discharge quantity table includes a plurality of remaining power levels, each of which is defined with respect to said system state and said power supply voltage.

Previous Doc Next Doc Go to Doc#

L8: Entry 6 of 7 File: USPT Oct 13, 1998

DOCUMENT-IDENTIFIER: US 5822198 A
TITLE: Single stage power converter and method of operation thereof

Abstract Text (1):
A single stage power converter has an energy storage device and is configured to receive electrical power. The single stage power converter includes: (1) an inductor, coupled to the energy storage device, for affecting a voltage across the energy storage device, (2) an asymmetrical half-bridge power circuit coupled to the energy storage device and having first and second power switches capable of being alternately activated to conduct current from the energy storage device to an output thereof and (3) a controller for controlling activation of the first and second power switches as a function of a characteristic of the output thereby to enhance a regulation of the output.

Brief Summary Text (13):
The single stage power converter including an energy storage device and couplable to a source of electrical power (e.g., an AC source of electrical power), includes: (1) an inductor, coupled to the energy storage device, for affecting a voltage across the energy storage device, (2) an asymmetrical half -bridge power circuit coupled to the energy storage device and having first and second power switches capable of being alternately activated to conduct current from the energy storage device to an output thereof and (3) a controller for controlling activation of the first and second power switches as a function of a characteristic of the output thereby to enhance a regulation of the output.

Brief Summary Text (16):
In a related embodiment of the present invention, the inductor is capable of storing energy from the source of electrical power during a first switching interval or first interval. The inductor is further capable of delivering energy to the energy storage device during a second switching interval or second interval. The inductor operates in a discontinuous conduction mode of operation to achieve power factor correction. In another related embodiment, the controller activates the first power switch during the first interval for a duty cycle (D) to provide a first conductive path between the source of electrical power and the inductor during the first interval. The controller further activates the second power switch during the second interval for a duty cycle (1-D) to provide a second conductive path between the inductor and the energy storage device during the second interval.

CLAIMS:

1. A single stage power converter including an energy storage device and couplable to a source of electrical power, comprising:

an inductor, coupled to said energy storage device, for affecting a voltage across said energy storage device;

an asymmetrical half-bridge power circuit coupled to said energy storage device and having first and second power switches capable of being alternately activated to conduct current from said inductor to said energy storage device and from said

energy storage device to an output of said power converter without requiring a switch between said energy storage device and said asymmetrical half-bridge power circuit; and

a controller for controlling activation of said first and second power switches as a function of a characteristic of said output thereby to enhance a regulation of said output.

4. The converter as recited in claim 3 wherein said controller activates said first power switch during said first interval for a duty cycle (D) to provide a first conductive path between said source of electrical power and said inductor, said controller further activating said second power switch during said second interval for a duty cycle (1-D) to provide a second conductive path between said inductor and said energy storage device.

8. A method of operating a single stage power converter including an energy storage device and couplable to a source of electrical power, comprising the steps of:

affecting a voltage across said energy storage device with an inductor;

alternately activating first and second power switches of an asymmetrical half-bridge power circuit, said first and second power switches conducting current from said inductor to said energy storage device and from said energy storage device to an output of said power converter without requiring a switch between said energy storage device and said asymmetrical half-bridge power circuit; and

controlling activation of said first and second power switches with a controller, said control being a function of a characteristic of said output thereby to enhance a regulation of said output.

15. A power supply, comprising:

an input for receiving an input AC voltage;

an input low-pass filter, coupled to said input, for filtering said input AC voltage;

an input rectifier, coupled to said input low-pass filter, for rectifying said input AC voltage; and

a single stage power converter including an energy storage device, comprising:

an inductor, coupled to said energy storage device, for affecting a voltage across said energy storage device,

an asymmetrical half-bridge power circuit coupled to said energy storage device and having first and second power switches capable of being alternately activated to conduct current from said inductor to said energy storage device and from said energy storage device to an output of said power converter without requiring a switch between said energy storage device and said asymmetrical half-bridge power circuit; and

a controller for controlling activation of said first and second power switches as a function of a characteristic of said output thereby to enhance a regulation of said output.

18. The power supply as recited in claim 17 wherein said controller activates said first power switch during said first interval for a duty cycle (D) to provide a first conductive path between said input and said inductor, said controller further activating said second power switch during said second interval for a duty cycle

L8: Entry 5 of 7 File: USPT Oct 19, 1999

DOCUMENT-IDENTIFIER: US 5966931 A
TITLE: Power supply control system for an electrically heated catalytic converter

Brief Summary Text (17):
This object is achieved by a power supply control system for an electrically heated catalytic converter according to one aspect of the present invention, which comprises an electric generator driven by an internal combustion engine, a battery, an electric heater for heating a catalytic converter disposed in an exhaust gas passage of the engine, a battery charging circuit which connects the battery with the generator and supplies an electric current for charging the battery, a catalyst heating circuit which directly connects the heater with the generator and supplies an electric current from the generator to the heater in order to raise the temperature of the catalytic converter to an activating temperature of catalysts in the catalytic converter, a temperature maintaining circuit which connects the heater with the battery and supplies an electric current from the battery to the heater in order to maintain the catalytic converter at the temperature higher than the activating temperature, first power supply control means for cutting off the battery charging circuit and the temperature maintaining circuit and closing the catalyst heating circuit when the engine has started, thereby heating the catalytic converter to the activating temperature, and second power supply control means for cutting off the catalyst heating circuit and closing the battery charging circuit and the temperature maintaining circuit when the temperature of the catalysts has reached the activating temperature, thereby charging the battery and, simultaneously, maintaining the catalytic converter at the temperature higher than the activating temperature.

Brief Summary Text (20):
According to another aspect of the present invention, there is provided a power supply control system for an electrically heated catalytic converter which comprises an electric generator driven by an internal combustion engine, an electric heater for heating a catalytic converter disposed in an exhaust gas passage of the engine, a battery connected to the generator, a catalyst heating circuit which connects the heater with the battery and supplies an electric current from the battery to the heater in order to raise the temperature of the catalytic converter to an activating temperature of catalysts in the catalytic converter, a temperature maintaining circuit which connects the heater with a neutral point of the windings of the generator and supplies an electric current from the neutral point to the heater in order to maintain the catalytic converter at the temperature higher than the activating temperature, first power supply control means for cutting off the temperature maintaining circuit and closing the catalyst heating circuit when the engine has started, thereby, heating the catalytic converter to the activating temperature, and second power supply control means for cutting off the catalyst heating circuit and closing the temperature maintaining circuit when the temperature of the catalysts has reached the activating temperature, thereby maintaining the catalytic converter at the temperature higher than the activating temperature.

L4: Entry 1 of 2 File: USPT Oct 2, 1984

DOCUMENT-IDENTIFIER: US 4475047 A
TITLE: Uninterruptible power supplies

Detailed Description Text (27):
The initial diagnostic routine, disclosed in flow chart form in FIG. 5, investigates the integrity of the power supply and its controls and is initiated when the power supply is initially activated. This diagnostic routine functions both before the power supply processes power and also, during operation of the power processing routines.

Detailed Description Text (89):
Routine zero, as indicated above, is always called in response to termination of the count down of the counter zero in the programmable interval timer. This can occur in two different ways. Normally, as described above, the counter zero is programmed with a first number (identified as 6600H above) so that the time of a complete count down of that word interval twice in a row is equal to the corresponding period of a 58 Hz sinusoidal signal. However, under normal circumstances, the word 6600H is not counted down two consecutive times. This first number is followed by 61A8H which is counted down subsequent to the 6600H value, when both numbers are consecutively and completely counted down, the termination of this total count down automatically calls for routine zero. Thus, during normal operating conditions when the AC signal is acceptable, the counter zero has not completed its count down of the two consecutive stored counts when the zero crossing of the primary AC input signal occurs. By reading the remaining count left therein at the zero crossing count down, the AC input frequency can be accurately calculated by one of the instruction routines and various control routines and words for other applications based on this calculated frequency can be, in turn, calculated. This count remainder, for example, provides a basis for calculating a timed interval approximately equal to a period of 22 1/2 degrees of the primary AC input signal used to generate the comb pulse waveform of counter one whose pulses occur at 1/16th the frequency of the primary AC input voltage. This generation of timing intervals shown by arrow 1107 in FIG. 15, which correspond to the leading edges of teeth pulses of the comb waveform 1120, determine the sampling intervals at which various power signals and states of the power supply are monitored by other instruction routines below. A zero crossing initiates routine one which immediately resets counter zero with the two aforedescribed standard count down words to begin a subsequent count down.

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L8: Entry 2 of 7 File: USPT Jul 17, 2001

DOCUMENT-IDENTIFIER: US 6262557 B1
TITLE: Motor with electronic distributing configuration

Abstract Text (1):
First power transistors of first power amplifying parts and second power transistors of second power amplifying parts form current paths from a DC power source to three-phase windings. A first distribution control block activates the first power amplifying parts with first three-phase signals, each having an active electrical angle larger than 120 degrees. A second distribution control block activates the second power amplifying parts with second three-phase signals, each having an active electrical angle larger than 120 degrees. A switching operation block has a current detecting part and a switching control part. The current detecting part obtains a current detected signal corresponding to a composed supply current of negative or positive parts of the three-phase drive currents to the three-phase windings. The switching control part compares an output signal of the current detecting part with a command signal and switches at least one power transistor of the first power transistors and the second power transistors to an off state when the output signal of the current detecting part becomes a value corresponding to the command signal, thereby causing the at least one power transistor to perform high-frequency switching responding with a comparison result.

Previous Doc Next Doc Go to Doc#

L8: Entry 3 of 7 File: USPT Dec 19, 2000

DOCUMENT-IDENTIFIER: US 6163187 A
TITLE: Charge pump circuit for phase locked loop free from spike current

Brief Summary Text (25):
In accordance with one aspect of the present invention, there is provided a charge pump circuit comprising an output node through which an output current and an input current flows, a current source connected to a first source of power voltage and flowing out a constant current, a first current mirror circuit having a first current path connected between the current source and a second source of power voltage different in potential level from the first source of power voltage, a second current path connected between the output node and the second source of power voltage and a first parasitic capacitor connected between a first control node for the second current path and the second source of power voltage, activated with a first control signal of an active level and responsive to a first potential at a first monitoring node between the current source and the first current path after the activation so as to vary a first current passing through the first current path and a second current passing through the second current path proportionally to one another, a second current mirror circuit having a third current path connected between the first source of power voltage and the output node, a fourth current path connected between the first source of power voltage and an intermediate node and a second parasitic capacitor connected between a second control node and the first source of power voltage, activated with a second control signal of an active level and responsive to a second potential at a second monitoring node between the fourth current path and the intermediate node after the activation so as to vary a third current passing through the third current path and a fourth current passing through the fourth current path proportionally to one another, a third current mirror circuit having a fifth current path connected between the constant current source and the second source of power voltage and a sixth current path connected between the intermediate node and the second source of power voltage and responsive to a third potential at a third monitoring node between the current source and the fifth current path so as to vary a fifth current passing through the fifth current path and a sixth current passing through the sixth current path proportionally to one another, a first switching circuit connected between the first control node and the second source of power voltage, and changed from an on-state to an off-state with the first control signal of the active level so as to charge the first parasitic capacitor through the first current path, and a second switching circuit connected between the second control node and the first source of power voltage, and changed from the on-state to the off-state with the second control signal of the active level so as to charge the second parasitic capacitor through the sixth current path.

L8: Entry 4 of 7 File: USPT May 30, 2000

DOCUMENT-IDENTIFIER: US 6069798 A
TITLE: Asymmetrical power converter and method of operation thereof

Brief Summary Text (16):
In one embodiment of the present invention, the asymmetrical power converter further includes a controller coupled to the first and second power switches. The controller alternately activates the first and second power switches to impress power from the input onto the isolation transformer. In a preferred embodiment, the controller activates the first power switch during a first interval for a first duty cycle (D) and alternately activates the second power switch during a second interval for a second duty cycle (1-D). The controller, therefore, monitors the output voltage and alternately activates the first and second power switches to regulate the output voltage.

Detailed Description Text (8):
The asymmetrical power converter 100 still further includes a controller 130 for controlling the switching cycles of the first and second power switches Q1, Q2. The controller 130 activates the first power switch Q1 during a first interval for a first duty cycle (D) to impress the first voltage V.sub.C1 across the first primary winding P1. The controller 130 then activates the second power switch Q2 during a second interval for a second duty cycle (1-D) to impress the second voltage V.sub.C2 across the second primary winding P2. The controller 130 monitors the output voltage Vout and activates the first and second power switches Q1, Q2 to regulate the output voltage Vout.

Detailed Description Text (9):
The asymmetrical power converter 100 operates as follows. During the first interval, the controller 130 activates the first power switch Q1 to impress the first voltage V.sub.C1 across the first primary winding P1. The first circulation path thus transfers power from the input of the asymmetrical power converter 100 to the isolation transformer T1. The first rectifying diode D1 conducts as current from the first output inductor L1 flows to the output through the first rectifying diode D1 and the output capacitor Co. Current in the second output inductor L2 flows to the output through the secondary winding S1, the first rectifying diode D1 and the output capacitor Co. Then, as the first interval ends, the controller 130 deactivates the first power switch Q1. Since the first power switch Q1 is now not conducting, a current in the first and second primary windings P1, P2 charges the intrinsic capacitance of the first power switch Q1. The intrinsic capacitance of the second power switch Q2 gradually discharges until a voltage across the second power switch Q2 is substantially zero. The controller 130 now activates the second power switch Q2 with substantially zero volts thereacross. A small delay period between the deactivation of the first power switch Q1 and the activation of the second power switch Q2 allows zero voltage switching (ZVS) to be employed to reduce voltage stress across the second power switch Q2.

Detailed Description Text (17):
The power supply 200 operates as follows. During the first interval, the controller 230 activates the first power switch Q1 to impress the first voltage V.sub.C1 across the first primary winding P1. Current in the output inductor Lo flows to the output through the output capacitor Co, the first secondary winding S1 and the

first rectifying diode D1. Then, as the first interval ends, the controller 230 deactivates the first power switch Q1. Since the first power switch Q1 is now not conducting, current in the first and second primary windings P1, P2 charges the intrinsic capacitance of the first power switch Q1. The intrinsic capacitance of the second power switch Q2 gradually discharges until a voltage across the second power switch Q2 is substantially zero. The controller 230 now activates the second power switch Q2 with substantially zero volts thereacross. A small delay period between the deactivation of the first power switch Q1 and the activation of the second power switch Q2 allows ZVS to be employed to reduce voltage stress across the second power switch Q2.

Previous Doc Next Doc Go to Doc#